Smart-Pixel Array for Imaging Sensors

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***Abstract*—This paper describes a CMOS smart-pixel array for applications in microchip size imaging sensor with pixel-level analog to digital conversion. This on-chip conversion is performed using a one-bit first-order sigma-delta converter for each pixel. The sensor outputs digital data in the form of bit streams containing information about the intensity of the incident light. The electronics circuits have been designed for occupying a very small chip area. Each pixel block consists of a photodiode and 19 mosfets. The sensor, the readout circuits and the digital interface are integrated on a single CMOS chip.**

I. INTRODUCTION

Charge Couple Devices (CCD) technology is robust for imaging applications and offers several charge-transfer architectures and specialized structural layouts. Usually, it is optimized for photodetection and features very low noise and a very high fill factor (the ratio of the photosensitive area to the total array area). CCD manufacturing outfits a number of technological issues in order to achieve high charge-transfer efficiency and to minimize crosstalk and noise. These issues increase the CCD fabrication complexity and cost. Furthermore, because of serial nature of the charge-transfer process, a conventional CCD does not feature random access to each pixel [1]. Typically, functional circuitry cannot be integrated reliably on-chip and when it is, the performance is poor, due to the difficulty of driving the large capacitive loads of the CCD, unless a combined CCD/CMOS process is meant, which clearly introduces relevant extra costs.

Applications that require imaging sensors would benefit if the analog to digital (A/D) conversion could be integrated with the image sensors in a single-chip. Advantages of such integration are lower power consumption, cost reduced, reliability improved and data conversion speed up. A single-chip require that all the components of an image sensor system are integrated on the same substrate, e. g., clock devices, image sensor, A/D conversion, control and signal processing. These requirements can be achieved by using a CMOS process. Besides being widely available, a standard CMOS process is generic, supports several photosensitive structures, favors the integration of multiple electronics functions with a high yield and it is, currently, the cheapest of the competing technology. If a standard technology for the fabrication of the image sensor system has to be followed, CMOS is a more sensible option due to its wide availability, reduced component and packaging costs and, more important, its capacity to accommodate multi-functional circuitry on-chip. Therefore, it stands as a reasonable choice for the fabrication of the proposed integrated image sensor system. However, standard CMOS is optimized for digital electronics and not for imaging. Consequently, it has a tendency to higher noise levels than CCD technology. Recent progress in on-chip signal processing allow the correction of fixed-pattern noise with negligible system impact, which has led to a reduction of CMOS image sensor fixed-pattern noise to acceptable levels [2].

II. SMART-PIXEL ARRAY DESIGN

A block diagram of the image sensor with pixel-level A/D conversion is shown in Fig. 1. Each block pixel comprises a photodetector and an A/D converter. A timing and control logic block is also integrated on-chip. This architecture allows several modes of image readout. Progressive-scan readout of the entire array is the common one. Readout of an interest area of the array, where only a smaller region of pixels is selected for readout or a random readout of each pixel is also possible. These modes increase access rates to interest areas of the array or allows for sub-sampling increasing readout speed. The columns addressing of the pixel array is performed using phase shifted clocks and, thanks to that, each pixel block of the same line can be connected to the same high-impedance output line, e. g., the N columns of the 1st line are connected to $Out1$. Each pixel block converts the incident light intensity into a digital code. The duty-cycle of the clock signal is $(1/N)\times 100\%$, where N is the number of pixel blocks in the columns.

Since a pixel-level A/D conversion is used, each A/D converter must be constructed using a very small silicon area. The A/D converter's size is inversely proportional to the number of pixels in the sensor and to the fill factor of each pixel. Conventional Nyquist A/D conversion techniques require too much silicon area to be viable for pixel A/D conversion. Therefore, oversampled A/D conversion based

Support for this research was provided by Engineering School (program IN²TEC) and R&D Centre Algoritmi of University of Minho.

on a sigma-delta converter provides a reasonable compromise between all requirements. This converter is very robust to process variation and system noise. Moreover, if it is a one-bit first-order sigma-delta converter, it can be performed with very little silicon area.

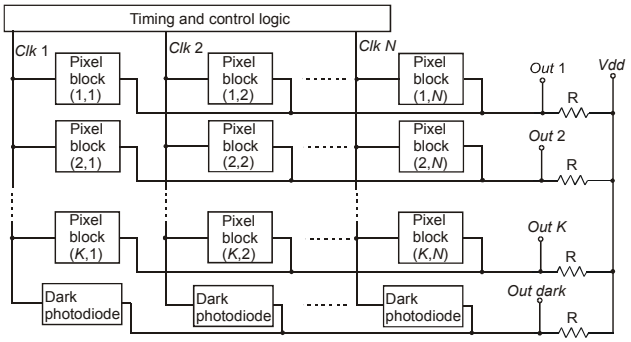

Figure 1. Image sensor chip functional block diagram.

A block diagram of the pixel block circuit is shown in Fig. 2. Initially, the integrators of the sigma-delta converters are reset to a known state by the global reset signal wire. Subsequently, an image is focused on the optical detectors and the sigma-delta converters start the conversion. Its results are read in all lines simultaneously. The oversampling frequency is set by the desired number of outputs bits (signal to noise ratio - SNR). Therefore, the oversampling principle allows a flexible trade-off between bandwidth and accuracy (noise). In this concrete application, since the input signal has no time variations and since the bandwidth allowed by the CMOS circuits is much higher than the required bandwidth for the light measurement, a one-bit first-order sigma-delta converter with an oversampling ratio of 128 or 256 can be used not at a so high-clock frequency. The digital values from the sigma-delta are reconstructed using a decimation filter, which can be programmed in a microcontroller.

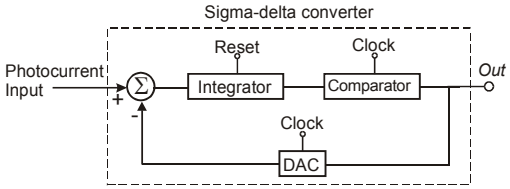

Figure 2. Pixel block.

III. PIXEL CIRCUITS AND OPERATION

A. Optical Detectors

The optical detectors convert the light intensity into a photocurrent. The photodetectors in the detector array must comply with standard CMOS capabilities. There are several possible photosensitive structures as vertical junction photodiodes in a standard *n-well* CMOS process [3]. These photodiodes are the *n-well*/*p-epilayer*, *n+*/*p-epilayer* and *p+*/*n-well* indicated in Fig. 3.

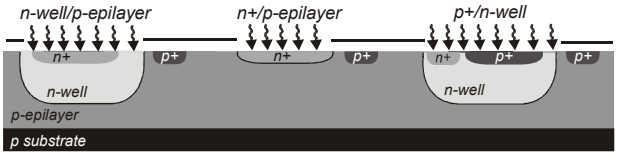

Figure 3. The three junction photodiodes in standard *n-well* CMOS.

For use in an array, the *p+*/*n-well* photodiodes are the least sensitive to substrate noise and crosstalk with neighboring pixels, because each junction is isolated within its own *n-well*. However, dense arrays cannot afford the huge separation required between two wells and, if electronic circuitry is to be added to each photodiode, the minimum distance between the *well* and the drain/source of a surrounding NMOS transistor must also be large enough to avoid latchup [4]. Equally, *n-well*/*p-epilayer* junctions transmit a large pitch on an array. This favors the *n+*/*p-epilayer* junction, where dense arrays are desired, with the disadvantages of higher crosstalk and lower sensitivity for longer wavelengths than the *n-well*/*p-epilayer* junction. Despite these disadvantages it has the higher quantum efficiency in the visible spectral range [5], due to the different doping concentration between the *n* and the *p* side, which extends the *p* side depletion area more deeply. The quantum efficiency indicates how well it collects the incident light and it is determined by intrinsic and extrinsic parameters. Intrinsic parameters are type of semiconductor, junction depth, depletion width and carrier diffusion length. However, there is little room to play with these parameters in standard CMOS. The most common extrinsic parameters are the stack of dielectric layers possibly left on top of the photodiode *pn*-junction and the pixel effective area (fill factor). In the standard double-metal CMOS process used, there are three dielectric layers above the *pn*-junction. Simulations show that the photodiode structure without two of those three dielectric layers provides the best possible quantum efficiency in the visible spectral range [6].

An additional photodiode for measuring the photodiode dark current is introduced in the circuit. The dark current density in standard CMOS is roughly one order of magnitude higher than that of conventional CCDs. An optimized CMOS process can feature a dark current density in the range between 50 and 200 pA/cm^2 (higher than the 1 pA/cm^2 obtained by specialized CCD imagers). Therefore, in the reported circuit, a dark current compensation channel is implemented in each column by a photodiode completely covered with metal. Since this current is temperature dependent, one measurement at the beginning of the data acquisition will not usually be enough, so, this current is measured and subtracted to the further data acquisitions.

B. Sigma-Delta A/D converter

A circuit schematic of the pixel block is shown in Fig. 4. The circuit consists of three main sections: the photodetector and the integrator, the comparator and the one-bit digital-to-analog converter (DAC). The integrator is based in a current mirror. It is initialized to a known state using mosfet *M3*. This initialization allows an improvement of 3 dB in the

SNR of the sigma-delta converter [7]. The photodiode current is integrated on the capacitor *C*. Since the integrator is based on a current mirror, the drain current of *M2* can be adjusted or amplified by changing only the *M2* size. Therefore, this circuit can work as an integrator with amplification. Its DC gain is given by the *M2* output resistance value, so, it is finite and higher than the oversampling ratio (detail can be found in [8]). At these conditions, the noise within the signal bandwidth only increases 0.3 dB [9]. Fig. 5 shows the simulated output voltage of the integrator for photocurrents of 3 nA and 100 nA. The graph shows clearly the effect of r_o in the output signal. However, even for the 100 nA curve, the fit can still be considered linear, once its Pearson coefficient is 0.9831.

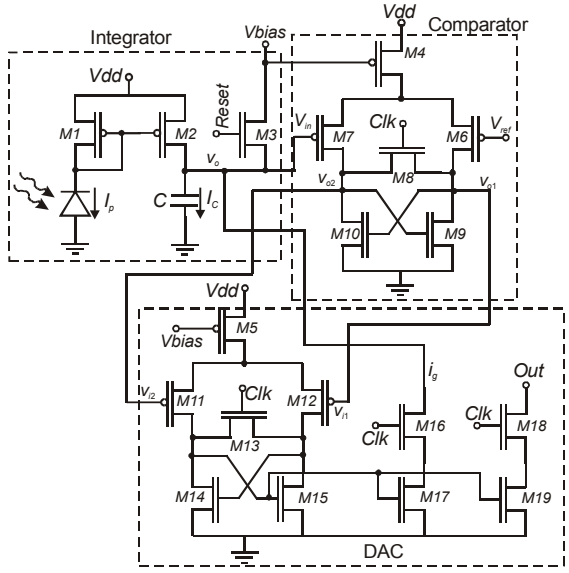

Figure 4. Pixel schematic.

The mosfets *M4* and *M5* provide the voltage bias of the circuit. Mosfets *M6* and *M7* form a matched differential pair that amplifies the voltage difference between the voltage on *C* and V_{ref} (the input reference voltage of the comparator). That difference is stored using the cross coupled pair *M9* and *M10*, which work like a latch, in the fall down clock transitions. The state of the latch is held while the clock signal is at low-level and *M8* is off. The performance of the comparator is shown in Fig. 6 for a $V_{ref} = 2.1$ V and a randomly chosen input voltage, v_{in}. This figure shows that at each fall down clock transition, the output voltage of the comparator goes up if $v_{in} < V_{ref}$ and goes down if $v_{in} > V_{ref}$.

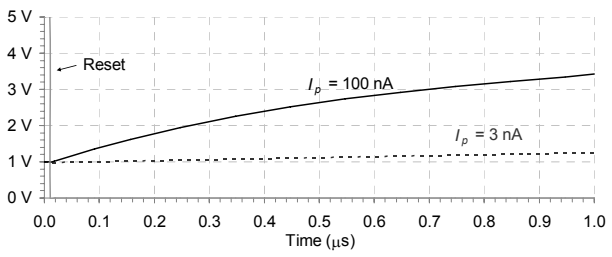

Figure 5. Integrator output voltage during one clock period.

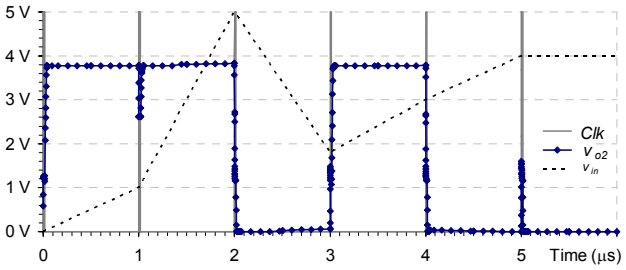

Figure 6. Performance of the comparator.

In the reported circuit, it is convenient to use a clock signal with a very low duty-cycle. There are two main reasons: the first one is the fact that during the comparison (at the high-level clock), the input signal must be approximately constant; the second one will be explained next.

Ideally, the gain of the comparator should be infinite, it should perform an almost rail-to-rail output (v_{o2} between 0 V and *Vdd*). However, from Fig. 6 it can be seen that its output is not rail-to-rail. Therefore, it was integrated in the DAC circuit another comparator stage (performed by the mosfets *M11* to *M15*), which allows increasing the global gain of the comparison. The mosfet *M17* converts the digital output level into a current that will discharge the capacitor, *C*, of the integrator, whenever it is necessary and during the high-level clock signal (performed by *M16*). After this clock period, the capacitor starts its charging until the integrator output reaches V_{ref}, and the cycle will be repeated. The duty-cycle of the clock and the voltage *Vbias* control the magnitude of the feedback signal current. Once the clock signal has a small duty-cycle, the capacitor is discharged during a small time, allowing the use of small capacitance values, which is a suitable requirement for being integrated in CMOS.

The global performance of the sigma-delta converter can be seen in Fig. 7, for a $V_{ref} = 2.8$ V and a sine wave photodiode current of $f = 5$ kHz with an amplitude of 60 nA. The output of each sigma-delta converter, *Out*, is obtained from this second stage comparator by the controlled current source formed by *M18* and *M19*. This output is activated only in the high-level clock being in a high-impedance state at the low-level. This means that with small duty-cycles clock signals, the number of the detectors in the array can be increased if the clock signals that address the columns on the array are shifted on time. In addition, the pixels of the same line can share the same output wire. For instance, with a clock duty-cycle of 1.5%, the array can comprise 64 columns sharing the same output wire, once each column pixel is read during a 1.5% of the clock period. This scheme avoids the need of a multiplexer/shift-register for pixel addressing.

Fig. 8 shows a detail of the performance of the 1st pixel line (*Out*1) for three columns, e.g., pixel block (1,1), (1,2) and (1,3), according to Fig. 1. The clock period is 1 µs with a 15 ns duty-cycle, allowing 64 pixel blocks columns, (smaller duty-cycles could be used for denser arrays). The detail of the output voltage, *Out*1 in Fig. 8e, shows when each pixel block is activated. The obtained number of frames/s was

about 4000, with 8 to 9 bits depth and 256 oversampling ratio.

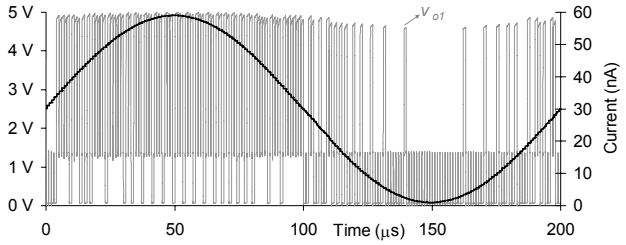

Figure 7. Waveforms of the sigma-delta converter working in closed loop: input current signal (I_p) and output voltage of the comparator (v_{o1}).

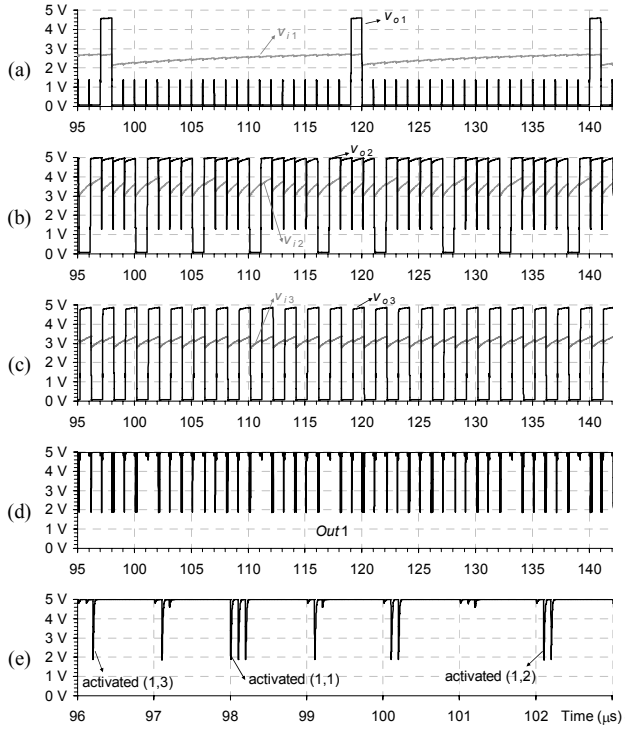

Figure 8. Waveforms of three sigma-delta converters placed in different addressing columns of the array (see Fig. 1): (a) integrator and comparator output voltage of pixel (1,1), for I_p = 3 nA; (b) integrator and comparator output voltage of pixel (1,2), for I_p = 60 nA; (c) integrator and comparator output voltage of pixel (1,3), for I_p = 30 nA; (d) output voltage *Out*1; (e) detail of the waveform presented in (d).

IV. SMART-PIXEL ARRAY FABRICATION

A microphotograph of the implemented chip is shown in Fig. 9. It has been fabricated through a 0.7 μm, double-metal, *n-well* CMOS process. Each photodiode has an active area of 100 μm × 100 μm. The sigma-delta converters were placed below the photodiodes. Each one has an area of 118 μm × 48 μm. The pixel blocks were surrounded with guard rings in order to minimize interference of stray carriers from the substrate. The measured photodiodes dark current was 96 pA/cm^2 at 0V.

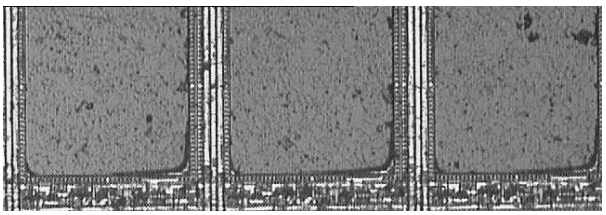

Figure 9. Microphotograph of three photodiodes with the corresponding A/D converters below.

V. CONCLUSIONS

Image sensors based on standard CMOS technology are gaining ground against CCDs, especially as the processes scale down further and special technological enhancements and new designs keep breaking performance barriers. A CMOS 64×64 smart-pixel array with pixel-level A/D conversion for imaging sensors was presented in this paper. Each pixel block comprises a CMOS photodetector and a sigma-delta converter, designed with only 19 mosfets. The image sensor outputs digital data in the form of a bit stream, which allows simple computer interfacing. Although the sigma-delta converters designed for this project have a very simple architecture, they have advantages relatively to other interfacing devices used for the same purpose, namely, the noise that is integrated with the signal and then digitally filtered, which means that, except for its small quantity in the signal band, it is eliminated by the device. Moreover, its relatively simple readout circuit and the compliance with a standard CMOS process (without extra masks) allow addition of this sensor to an existing CMOS design. The simulation results have shown a promising performance, not only for this particular application, but for all applications where an array of photodetectors must be read. Meanwhile, the measurement and test setup are being developed for obtaining the so desired experimental results.

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